AMENDMENTS TO THE CLAIMS

Claims 1-64 (Cancelled).

65. (Currently Amended) A method of forming a conductor on a semiconductor structure, the semiconductor structure having a layer of insulation material and a via that contacts the layer of insulation material, the layer of insulation material having a top surface, the method comprising:

etching the top surface of the layer of insulation material to form a plurality of spaced-apart first openings in ~~the top surface of~~ the layer of insulation material, each first opening having a bottom surface that lies below the top surface of the layer of insulation material; and

simultaneously etching the top surface of the layer of insulation material and the bottom surface of each first opening to form a second opening in ~~the top surface of~~ the layer of insulation material, and lower the bottom surface of each first opening to form a plurality of spaced-apart lowered first openings that ~~expose~~ each have a bottom surface, the bottom surfaces of two or more of the plurality of spaced-apart lowered first openings exposing the via, the second opening having a top that lies in a common plane with the top surface of the layer of insulation material ~~and includes no portion of the top surface of the layer of insulation material~~, and a bottom that lies below the top surface of the layer of insulation material, each of the plurality of spaced-apart lowered first openings extending away from the bottom of the second opening.

66. (Previously Presented) The method of claim 65 wherein the bottom surface of a lowered first opening exposes an area of the via and an area of the insulation material, the area of the insulation material that is exposed being substantially greater than the area of the via that is exposed.

67. (Previously Presented) The method of claim 65 wherein the bottom surface of each lowered first opening exposes an area of the via and an area of the insulation material, the area of the insulation material that is exposed being substantially greater than the area of the via that is exposed.

68. (Previously Presented) The method of claim 65 and further comprising:

depositing a conductive material on the top surface of the layer of insulation material to fill up the second opening and the plurality of spaced-apart lowered first openings; and

removing the conductive material from the top surface of the layer of insulation material so that a top surface of the conductive material and the top surface of the insulation region lie approximately in a common plane to form a conductive region, the conductive region having a first region that lies in the second opening, and a plurality of spaced-apart second regions that lies in the plurality of spaced-apart lowered first openings to extend away from the first region, each second region contacting the via.

69. (Currently Amended) A method of forming a conductor on a semiconductor structure, the semiconductor structure having a layer of insulation material and a contact that touches the layer of insulation material, the layer of insulation material having a top surface, the method comprising:

etching the top surface of the layer of insulation material to form a plurality of spaced-apart first openings in ~~the top surface of~~ the layer of insulation material, each first opening having a bottom surface that lies below the top surface of the layer of insulation material; and

simultaneously etching the top surface of the layer of insulation material and the bottom surface of each first opening to form a second opening in ~~the top surface of~~ the layer of insulation material, and lower the bottom surface of each first opening to form a plurality of spaced-apart lowered first openings that ~~expose~~ each have a bottom surface, the bottom surfaces of two or more of the plurality of spaced-apart lowered first openings exposing the contact, the second opening having a top that lies in a common plane with the top surface of the layer of insulation material ~~and includes no portion of the top surface of the layer of insulation material~~, and a bottom that lies below the top surface of the layer of insulation material, each of the plurality of spaced-apart lowered first openings extending away from the bottom of the second opening.

70. (Previously Presented) The method of claim 69 wherein the bottom surface of a lowered first trench exposes an area of the contact and an area of the insulation material, the area of the insulation material that is exposed being substantially greater than the area of the contact that is exposed.

71. (Previously Presented) The method of claim 69 wherein the bottom surface of each lowered first opening exposes an area of the contact and an area of the insulation material, the area of the insulation material that is exposed being substantially greater than the area of the contact that is exposed.

72. (Previously Presented) The method of claim 69 and further comprising:

depositing a conductive material on the top surface of the layer of insulation material to fill up the second opening and the plurality of spaced-apart lowered first openings; and

removing the conductive material from the top surface of the layer of insulation material so that a top surface of the conductive material and the top surface of the insulation region lie substantially in a common plane to form a conductive region, the conductive region having a first region that lies in the second opening, and a plurality of spaced-apart second regions that lies in the plurality of spaced-apart lowered first openings to extend away from the first region, each second region touching the contact.

73. (Currently Amended) A method of forming a conductive line on a semiconductor structure, the semiconductor structure having a layer of insulation material, the layer of insulation material having a top surface, the method comprising:

etching the top surface of the layer of insulation material to form a plurality of spaced-apart first trenches in ~~the top surface of~~ the layer of insulation material, each first trench having a bottom surface that lies below the top surface of the layer of insulation material, a first width, and a first length that is substantially greater than the first width; and

simultaneously etching the top surface of the layer of insulation material and the bottom surface of each first trench to form a second trench in ~~the top surface of~~ the layer of insulation material, and lower the bottom surface of each first trench to form a plurality of spaced-apart lowered first trenches, the second trench having a top that lies in a common plane with the top surface of the layer of insulation material ~~and includes no portion of the top surface of the layer of insulation material~~, a bottom that lies below the top surface of the layer of insulation material, a second width, and a second length that is substantially greater than the second width, each of the plurality of spaced-apart lowered first trenches extending away from the bottom of the second trench and having a third width and a third length that is substantially greater than the third width.

74. (Previously Presented) The method of claim 73 wherein the plurality of spaced-apart lowered first trenches lie substantially parallel to each other.

75. (Previously Presented) The method of claim 73 wherein the second and third lengths are approximately equal.

76. (Previously Presented) The method of claim 73 and further comprising:

depositing a conductive material on the top surface of the layer of insulation material to fill up the second trench and the plurality of spaced-apart lowered first trenches; and

removing the conductive material from the top surface of the layer of insulation material so that a top surface of the conductive material and the top surface of the insulation region lie substantially in a common plane to form a conductive trace, the conductive trace having a first region that lies in the second trench, and a plurality of spaced-apart second regions that lies in the plurality of spaced-apart lowered first trenches to extend away from the first region.

77. (Previously Presented) The method of claim 76 wherein the conductive trace is formed to have a number of loops that lie substantially in a same plane.

78. (Previously Presented) The method of claim 73 wherein the bottom surface of a lowered first trench exposes an area of a conductive region and an area of the insulation material, the area of the insulation material that is exposed being substantially greater than the area of the conductive region that is exposed.

79. (Previously Presented) The method of claim 73 wherein the bottom surface of each lowered first trench exposes an area of a conductive region and an area of the insulation material, the area of the insulation material that is exposed being substantially greater than the area of the conductive region that is exposed.

80. (Previously Presented) The method of claim 73 wherein the second trench has an approximately uniform width.